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A Reliable LDMOS Transistor Based on GaN and Si_3N_4 Windows in Buried Oxide

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A R T I C L E I N F O

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A B S T R A C T

High breakdown voltage and reduced specific on-resistance are obtain in the new LDMOS structure with wide band gap material in the buried oxide. GaN with higher mobility and wider band gap energy than silicon is an important material that causes better performance in power devices. Moreover, self-heating effects of the proposed LDMOS structure is controlled using two other Si_3N_4 windows at the top and bottom of the GaN window. Our simulation with two-dimensional ATLAS simulator shows that the proposed three windows in buried oxide of the LDMOS transistor (TW-LDMOS) has better reliability than conventional LDMOS (C-LDMOS) structure due to the flexible behavior of the TW-LDMOS in higher drain voltages and reduced electron temperature.

1. Introduction

The application of the power MOSFETs are became extensive in recent technology[1-4]. New devices and switches are introduced to work in high voltages[5].Also, he challenges in power electronic devices are achieving high breakdown voltage and low specific on-resistance[6-8].Obtain the acceptable values for these parameters in the same time are complicated[9].But recently new devices are introduced to have better behavior [10-13]. In these structures new techniques like using different windows in the drift region, using different materials in the channel region and modified buried oxide are applied to improve the performance of lateral double diffused metal oxide semiconductor transistors (LDMOSs) [14]. Increasing the length of the drift region is another important way to increasing breakdown voltage but the specific on-resistance increases in such devices.

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In another point of view, SOI technology is known as an effective way for controlling drawbacks of leakage current, body effect and leakage capacitance in the MOSFETs [15]. But the buried oxide in the middle of the structure increases the temperature in the active region and the self-heating effects occurs [16]. In order to control the self-heating effects on the performance of the device, using different windows under the channel region is effective.

In this paper we have proposed a new structure of the LDMOS transistor in which we have used wide band gap material as a window in the buried oxide under the drift region. Two other windows with Si_3N_4 materials are applied to have an effective way for transferring the heat from the active region to the substrate. Wide band gap materials are important in power transistors to have high breakdown voltage and high switching speed. Moreover, by controlling the electric field profile we can have reliable device. Modified electric field causes to control the peaks of the electric field at the interfaces. So, the electrons could not reach the maximum values and the hot electron effects reduce, significantly.

Our simulation with two-dimensional ATLAS simulator shows that the proposed three windows in the buried oxide of LDMOS transistor has acceptable results in comparison to C-LDMOS transistor [17].

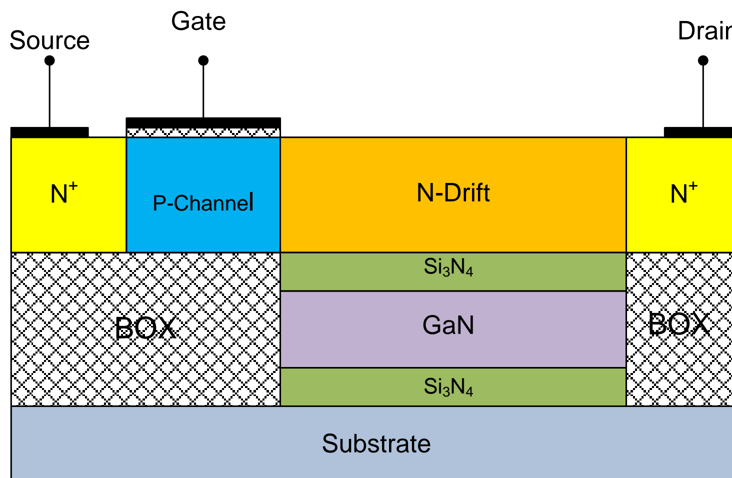

Fig. 1. Schematic crosssection of the proposed LDMO structure.

Fig. 1 shows the schematic of the proposed structure with three windows in the buried oxide of the LDMOS transistor. As it is clear in this figure two Si_3N_4 layers and a GaN windows are located under the drift region of the structure. The Si_3N_4 layers have lower thicknesses while the GaN window is thicker. In order to have simple fabrication processes in the proposed structure, the lengths of the windows are equal to the drift region length. In this new structure only one extra mask is needed for creation of the windows. Also, the three windows in the buried oxide of the LDMOS (TW-LDMOS) is simulated using two-dimensional ATLAS simulator and the results are compared to the C-LDMOS transistor. In the simulation we have used CCSMOB, FLDMOB, SHR, ANALYTIC models to obtain accurate results [18]. Moreover, AUGER and IMPACT SELB are applied for the recombination and impact ionization mechanisms in the simulator. Likewise, carrier velocity saturation, carrier-carrier scattering at high doping and the dependence of the mobility on temperature and transverse electric field are considered in the simulation. All

the parameters which are used in the simulation of the TW-LDMOS structure are given in Table I. it is important to note that the conventional structure has the same parameters values for the simulation only these three windows are not considered in the buried oxide.

Table 1. Device parameters used in the ATLAS simulation.

Device Parameters	**TW-LDMOS**
Channel length	7μm
Drift length	10 μm
GaN length	10 μm
D/S length	2μm
BOX thickness	500 nm
Gate oxide thickness	20 nm
GaN thickness	200 nm
Si_3N_4 length	10 μm
Si_3N_4 thickness	100 nm
Channel doping density	5×10^{16} cm^{-3}
S/D doping density	1×10^{19} cm^{-3}
Drift doping density	1×10^{17} cm^{-3}
Substrate doping density	1×10^{14} cm^{-3}

2. Results and Discussion

The main purpose of the TW-LDMOS structure is considering GaN as a window in the buried oxide. This material has wide band gap energy that improves the application of devices in the power switches. The other advantages of the GaN over silicon is higher mobility and higher critical electric field value. in Fig. 1 the electric field along channel is plotted. As the figure shows the C-LDMOS reaches the maximum value of the electric field at the x=7 μm while the TW-LDMOS have lower values in the all positions in the channel. The physical reasons of this behavior are due to the locating three windows in the buried oxide that reduces the main peak of the electric field in the channel region. Also, GaN material has higher critical electric field value which causes flexible electric field in the high drain voltages. So, two main results will be happened by modified electric field profile in the TW-LDMOS transistor. One of them is higher breakdown voltage of the proposed structure than C-LDMOS. As the Fig. 3 shows, the breakdown voltages in the different drift lengths of the TW-LDMOS have higher values. So, the application of such devices in the power electronic becomes effective. The other result is reduced electron temperature of the TW-LDMOS transistor that we have studied this parameter later.

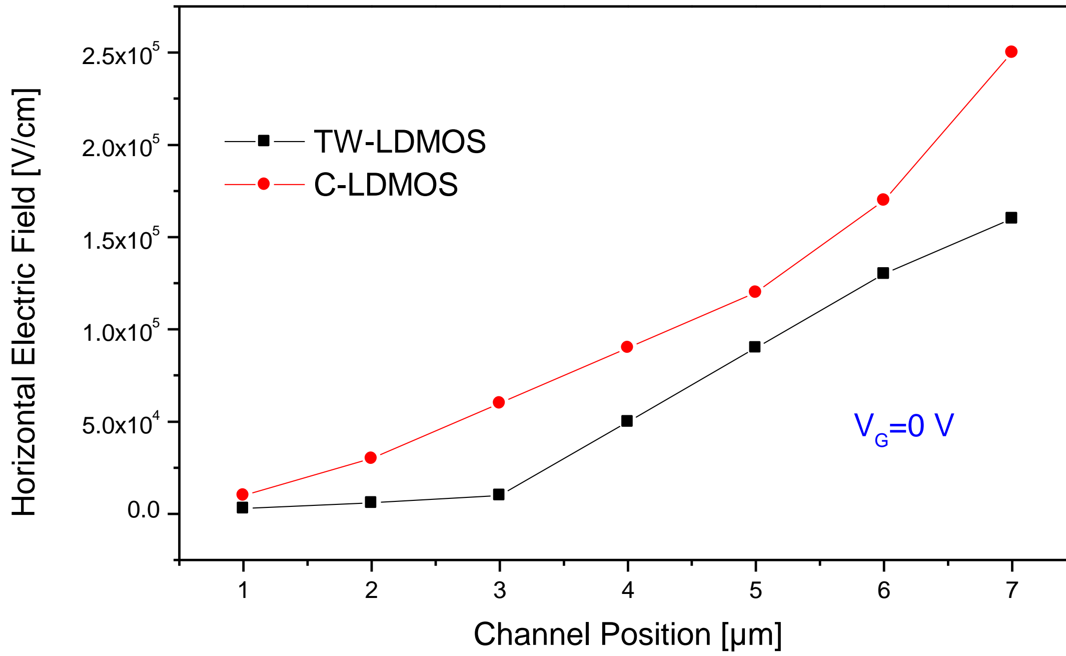

Fig. 2. Electric field profiles of the proposed structure and conventional one.

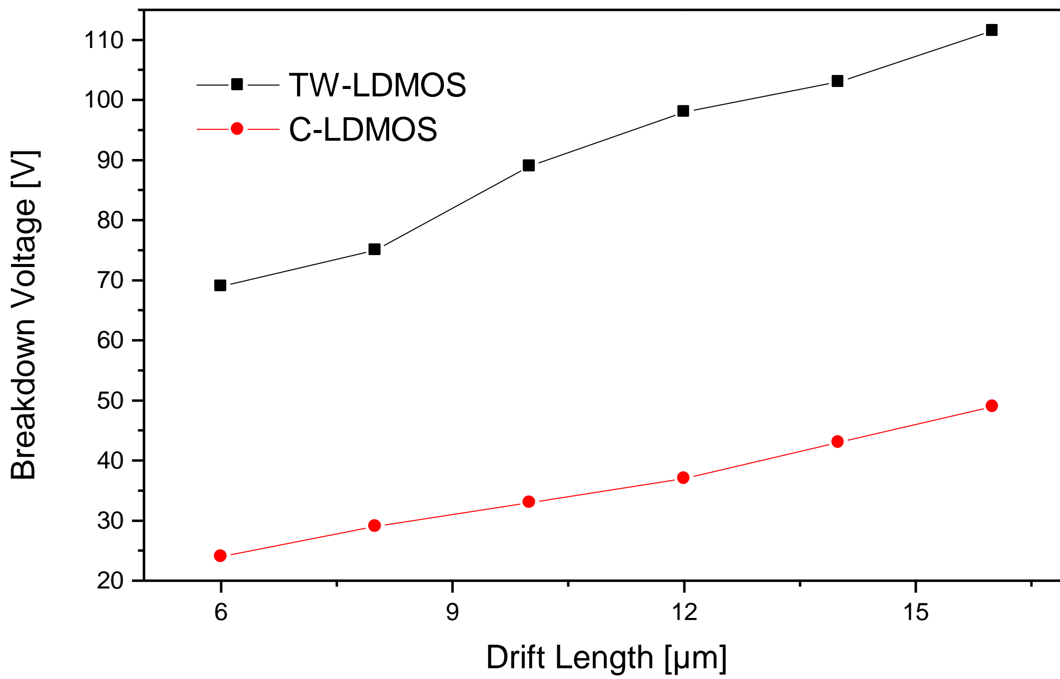

Fig. 3. Breakdown voltage versus drift length for the TW-LDMOS and C-LDMOS transistors.

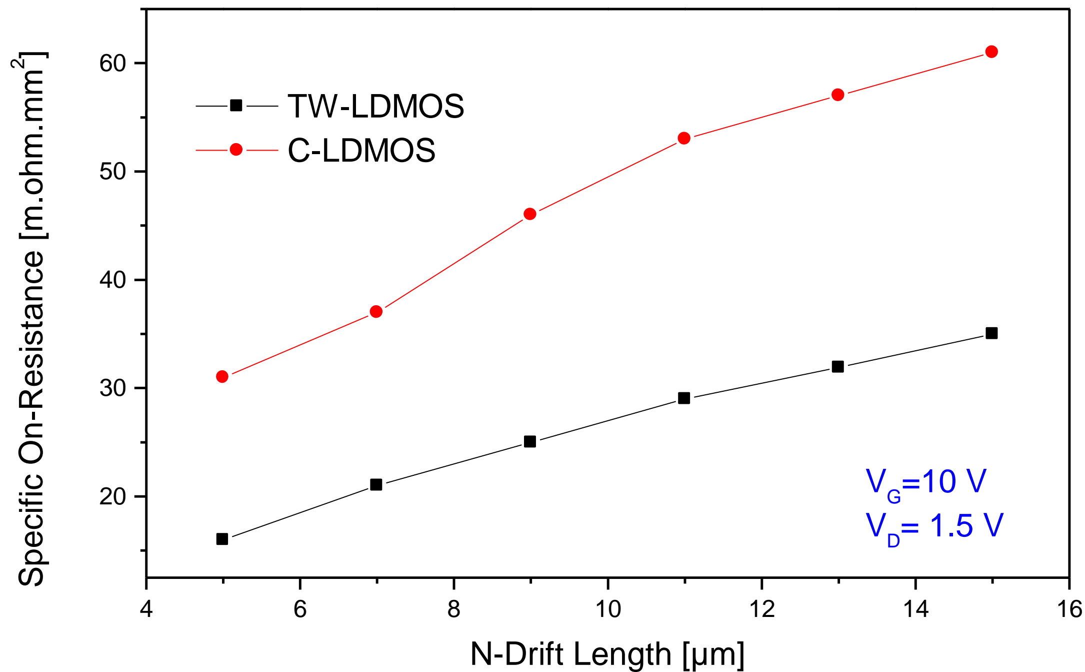

Fig. 4. Specific on-resistance is compared for the proposed structure and conventional one at the gate bias of 10 V.

GaN is important to achieve lower specific on-resistance in the device. Wide band gap of the GaN is effective for switching characteristic. In this situation on-resistance will be reduced that causes sharp on to off converting. Moreover, the speed of switching increases by applying GaN in the device. In the Fig. 4 the specific on-resistance versus drift region length is compared for the both structures in this study. In all lengths lower specific on-resistance of the TW-LDMOS structure is clear.

Electron temperature is one of the parameters for evaluation of the reliability in different devices. In the proposed TW-LDMOS, using Si_3N_4 and GaN windows help to have modified electric field that do not reach the maximum values at the interface of the channel/source and channel/drift regions. So, the electrons could not obtain the maximum energy that leads to lower electron temperature. This effect which is named as hot electron effect is controlled in the proposed structure, significantly. In Fig. 5 the electron temperature of the TW-LDMOS is simulated for two different GaN thicknesses. The figure shows that increasing the thickness of the GaN is effective to achieve lower electron temperature. Higher electron mobility of GaN and critical electric value of this material are important to have reliable device. It is important to note that the C-LDMOS has higher value of electron temperature than the proposed structure.

In order to determine the effective role of the Si_3N_4 on the self-heating effect, we have measured the temperature of the two devices in the drift region. The exact point for this measurement is x=14µm and y= 0.2 µm. The results are compared in the Table II for different Si_3N_4 thickness of the TW-LDMOS and also for C-LDMOS.

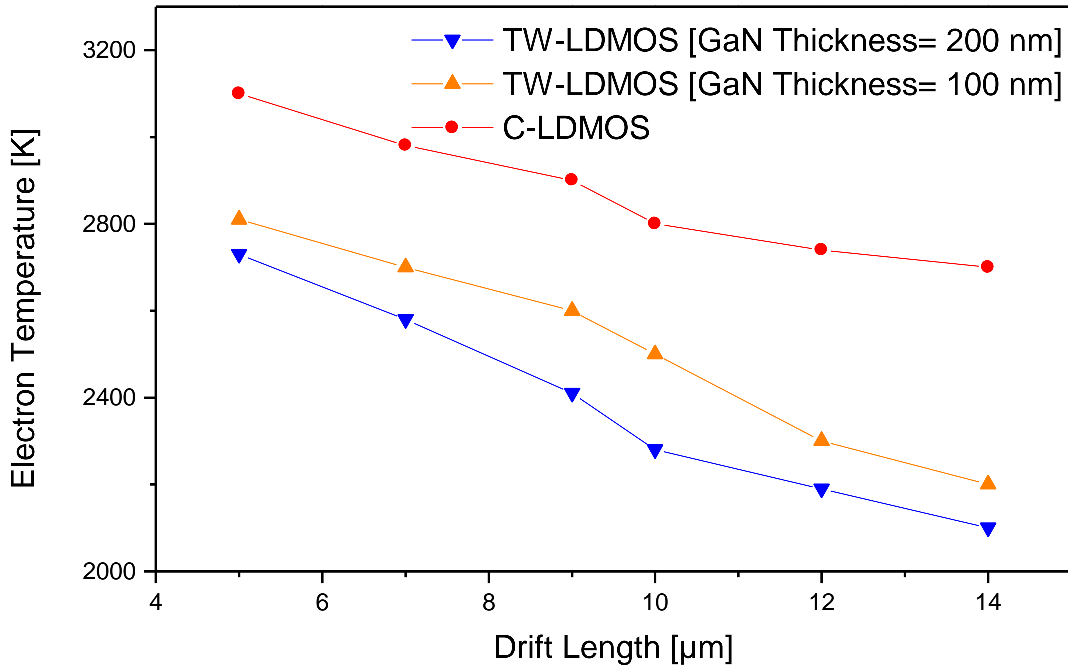

Fig. 5. Electron temperature of the TW-LDMOS in two different GaN thicknesses and C-LDMOS are compered.

Table 2. TW-LDMOS and C-LDMOS temperatures in the drift region.

Device	**Temperature (K)**
TW-LDMOS (Si_3N_4 thickness 50 nm)	319
TW-LDMOS (Si_3N_4 thickness 100 nm)	315
TW-LDMOS (Si_3N_4 thickness 150 nm)	312
C-LDMOS	360

3. Conclusion

A new LDMOS structure using GaN window as a wide band gap material and two Si_3N_4 windows are proposed in this paper. A GaN window is effective to have higher breakdown voltage and reduced specific on-resistance. Moreover, two Si_3N_4 are used for transferring heat from the active region to the substrate to control self-heating effect. Our simulation with two-dimensional ATLAS simulator shows that the proposed structure modified the electric field and reduces the electron temperature in the high voltages. So, the reliability of this novel structure is more than conventional LDMOS transistor.

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