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Design and Optimization of 0.18µm CMOS Operational Amplifier for Use in High Frequencies Applications used Invasive Weed Optimization (IWO) algorithm

Salih Mahdi Kadhom [a], Daryoosh Dideban [a,*], Hassan Jassim Motlak [b]

[a] Department of Electronics, Faculty of Electrical and Computer Engineering, University of Kashan, Kashan, Iran

[b] Deparment of Engineering, University of Babylon, Iraq

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ABSTRACT

Day after day, the need for a high-performance CMOS OP-AMP is increasingly needed for use in electronic and communications applications as well as in the biomedical field. For this purpose, OP-AMP must operate at wide band-width and high voltage gain with low power consumption. To design a high-performance OP-AMP we must select a modern technology in order to harmonize the process parameters of MOSFET transistors with the technique of the proposed CMOS OP-AMP consisting of a group of these transistors. In this paper, 0.18µm TSMC technology with ±1.8V supply voltage CMOS-OP-AMP is used to design Two Stage OP-AMP. Simulation results are obtained using PSPICE (version 16.6.0) program. The results showed that the designed techniques are highly efficient in terms of high frequency, high gain and low consumption of power. The Invasive Weed Optimization (IWO) algorithm was used to improve the performance parameters of the Two-Stage CMOS OP-AMP, and it implemented with MATLAB program. The simulation results of the proposed OP-AMP based-on IWO algorithm showed the GBP is improved into 100%, the voltage gain increased around 17% , the power consumption decreased by 32% and CMRR increased by 20% .From the result we can say that the IWO is a powerful algorithm can be used to improve other designs.

1. Introduction

The low cost of manufacture and the possibility of placing both analog and digital circuits on the same chip in order to improve the whole performance and decrease the cost of packaging made CMOS technology desirable. The intrinsic speed of MOS transistors has increased by orders of

* Corresponding author.
E-mail addresses: dideban@kashanu.ac.ir (D. Dideban)

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magnitude in the past 67 years, exceeding that of bipolar devices even though the latter have also been scaled (but not as fast). Also the dimensions of MOS devices can be scaled down more easily than those of other types of transistors, Furthermore, consume low power. The next obvious step was to apply CMOS technology to analog design.

In today's technology, CMOS circuits run from supplies around 1 V and bipolar circuits around 2V.The Lower supplies have been permitted consumption a low power in the integrated circuits [1].

At the beginning , most Op-Amps were designed to serve as " general purpose" building blocks, Meets the requirements of many different Implementations, and this led to create an " ideal" Op-Amp (high voltage gain, high input impedance and low output impedance), at the expense of other specifications such as speed, output voltage swing and power dissipation. Today's become it is necessary to know the optimum value that must be achieved for each parameter to design successful op-amp [1,3].

Beside the gain and speed, there is another important parameters such as power dissipation, supply voltage, linearity, noise, and the maximum output voltage swings. Also the input and output impedances determine how the circuit interacts with the previous and next stages and work together (jointly) [1].

With reduce the channel length and low power applications the designing of Op-Amps creates new challenges, but with advancements of the new techniques, there are more options to solve this problem. In some applications the cascade Op-Amps may not be sufficient to produce the enough gain and the required output swings, in such cases, we must choose another topology. One solution is "Two Stage" Op-Amp, with the first stage providing a high gain and the second stage gives us large swing. In Two Stage CMOS Op–Amps because of there are two dominant poles, the phase margin could easily reach to a value less than that enough for stable operation, so the designers should be taken into account this serious problem, otherwise there is a good chance that the Op-Amp will oscillate and instead of an amplifier it will act as an oscillator [2,3].

2. Design Parameters and simulation results of basic two stage Op-Amp

The basic schematic of the two stage op-amp is illustrated in Fig.1. The design parameters and specifications as well as transistor dimensions are presented in Tables 1, 2, respectively. The implemented SPICE schematic is given in Fig.2.

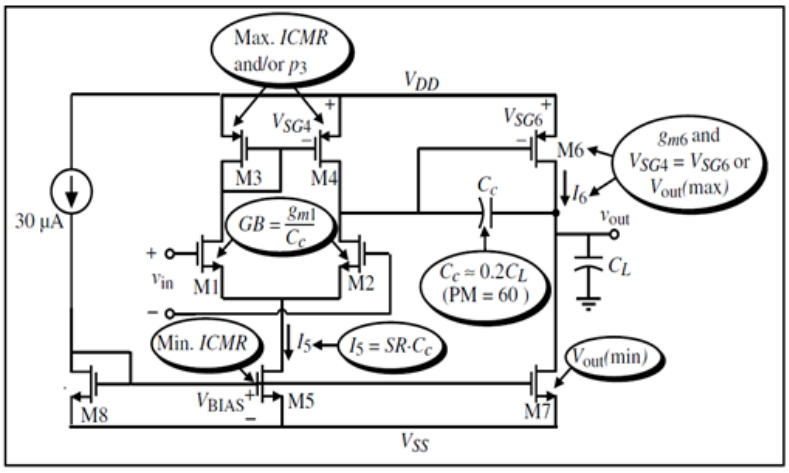

Figure. 1. Circuit& design relationship for two Stage CMOS Op-Amp.

Table 1. Specifications of proposed two Stage CMOS Op-Amp with 30 µA biasing current

Design Parameters	Values with units
DC Gain	>60 dB
Gain Bandwidth	>40MHz
Slew Rate	>20 V/µsec
Supply Voltage(V_{DD}, V_{SS})	±1.8V
Input Common Mod Range	-1 to+ 1.65 V
Phase Margin	≥ 55 °
Load Capacitor	3 pF
I_{bias}	30uA

Table 2. Summarized gate dimensions of proposed Two Stage CMOS with 30 µA biasing current.

Transistor number	Type	Gate width (µm) W	Channel length L (µm)
M1 , M2	N	2.4	0.18
M3 , M4	P	1.54	0.18
M5 , M8	N	1.09	0.18
M6	P	21.39	0.18
M7	N	7.4	0.18

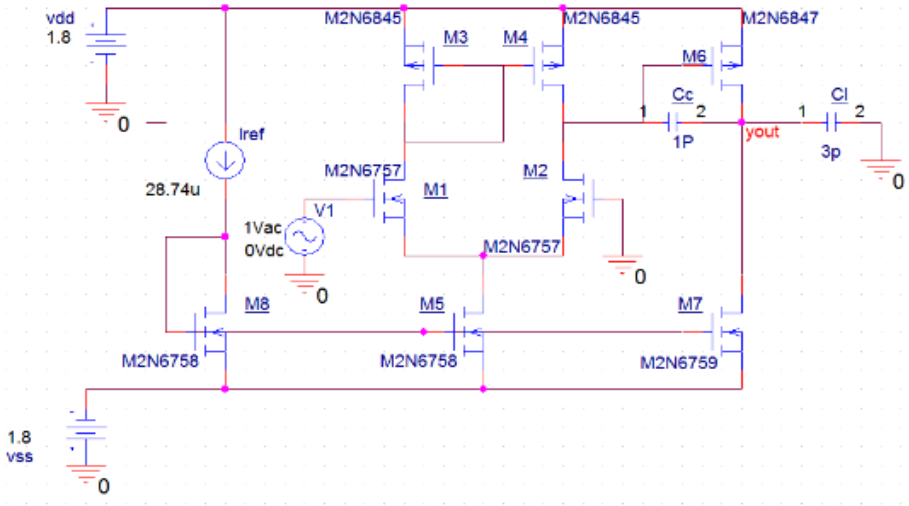

Figure. 2. Practical circuit diagram for the Two Stage CMOS Op-Amp

3. Simulation Results

The circuit gain measurement results are simulated and shown in Figs. 3,4, for the amplitude and phase, respectively. Table 3 presents the effects of change the value of C_L on the performance parameters of the two stage CMOS Op-Amp.

The impact of change of load capacitance (C_L) on the unity gain-band width (UGB) and phase margin of the proposed Op-Amp are shown in Figs. 5,6, respectively. Fig. 7 depicts the practical circuit of two stage Op-Amp connected as a buffer used to test the value of slew rate and settling time. The simulation results for the slew-rate (SR) and settling-time (ts) are given in Figs. 8,9, respectively. Finally, Figs. 10, 11 show the configuration and simulation results for CMRR of basic two stage op-amp under our study.

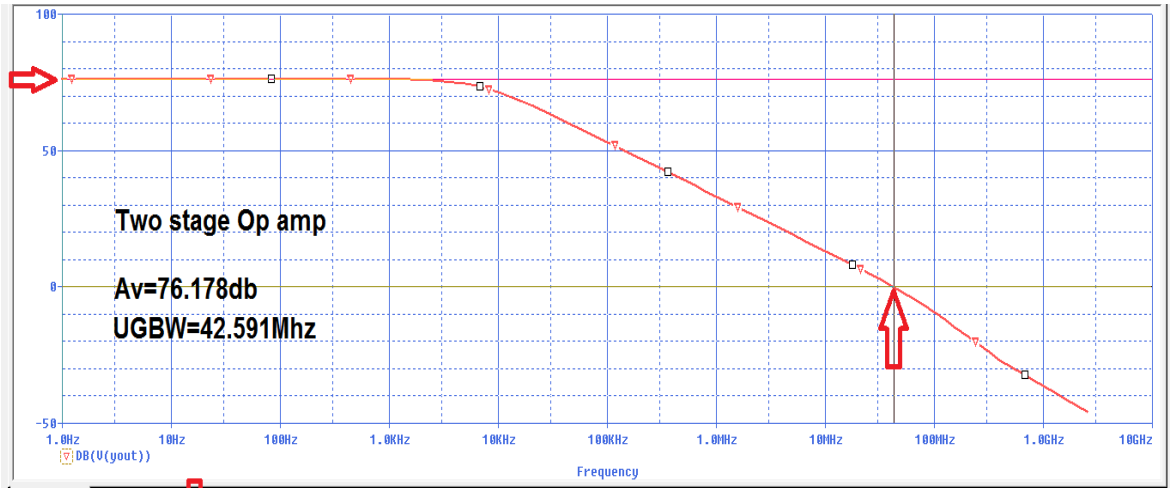

Figure. 3. Simulation result (Gain measurement)

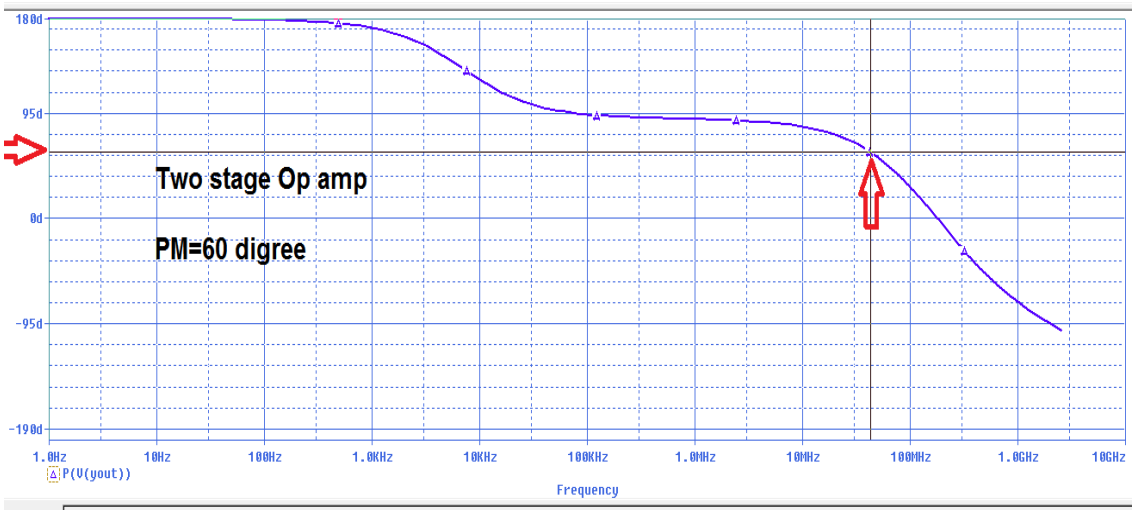

Figure. 4. Simulation result (Phase measurement)

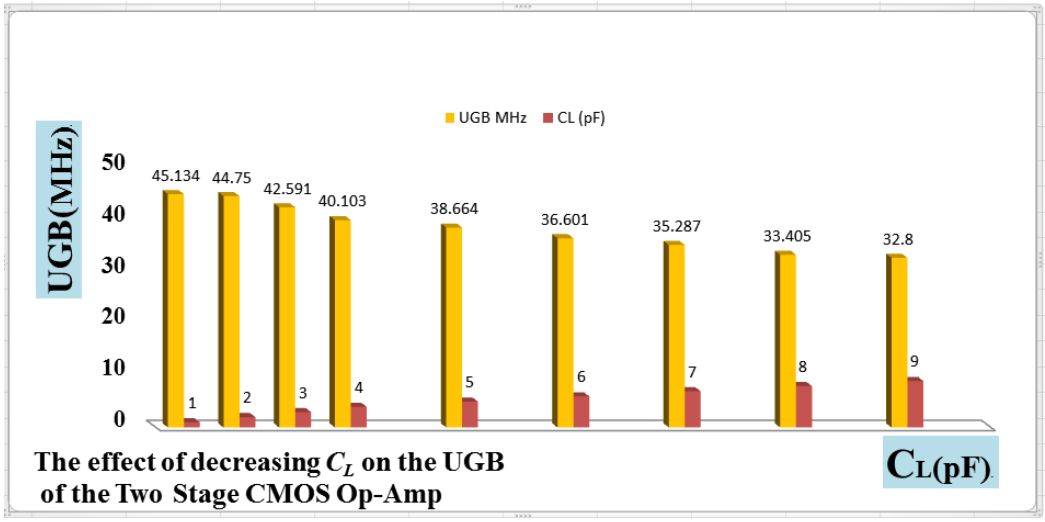

Figure. 5. The effects of change the value of C_L on the UGB

Table 3. The effects of change the value of C_L on the performance parameters of the two stage CMOS Op-Amp

C_L pF	UGB(MHz)	PM (degree)	Av (dB)
1	45.134	73.275	78
2	44.75	65.640	78
3	42.591	60.0	78
4	40.103	56.018	78
5	38.664	51.571	78
6	36.601	49.530	78
7	35.287	46.650	78
8	33.405	45.010	78
9	32.80	42.602	78

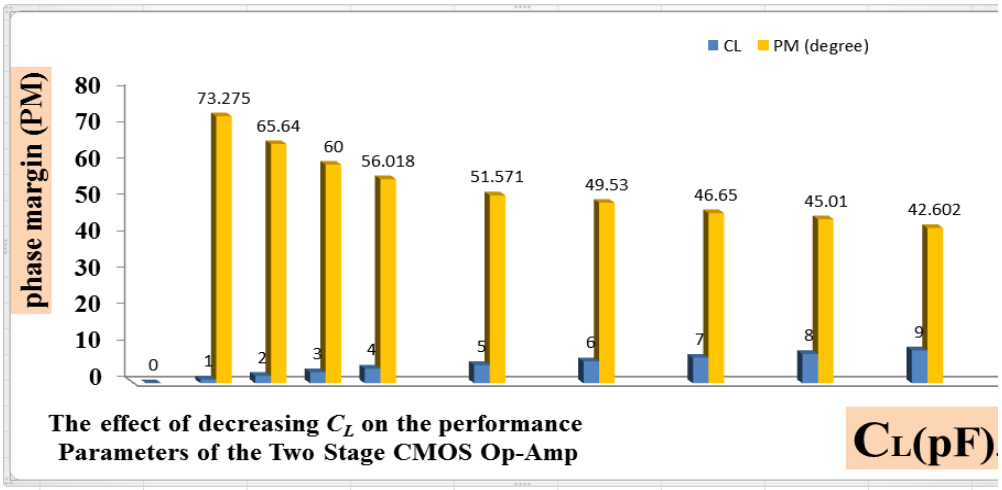

Figure. 6. The effects of change the value of C_L on the phase margin

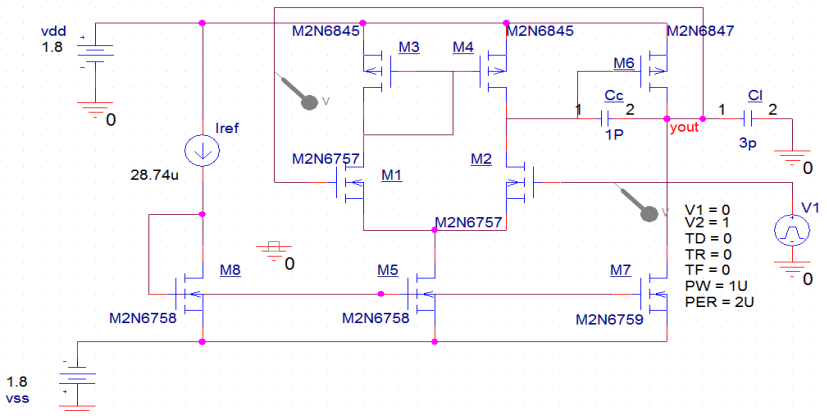

Figure. 7. The practical circuit of two stage Op-Amp connected as a buffer used to test the value of slew rate and settling time.

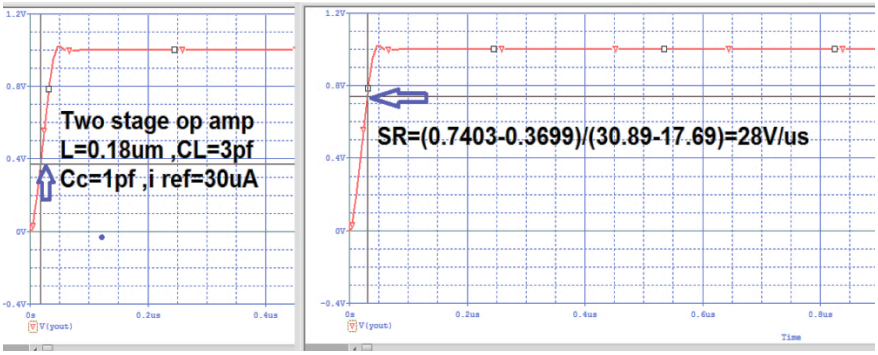

Figure. 8. Simulation result of measurement of Slew Rate (SR).

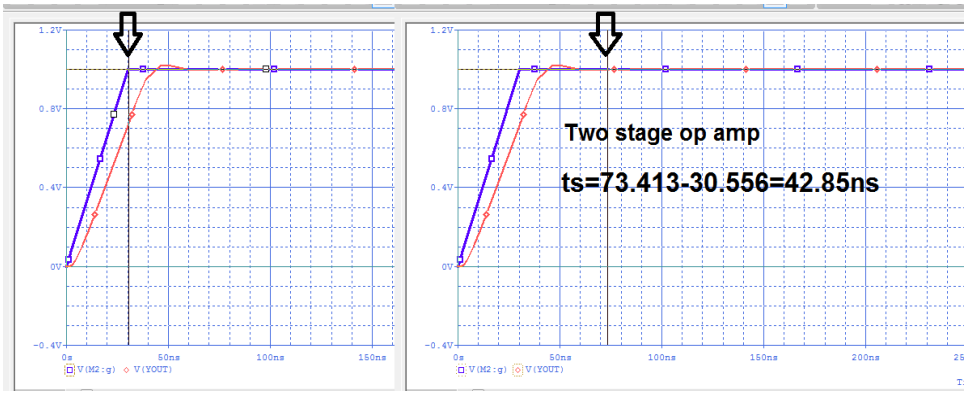

Figure. 9. Simulation result of settling time **(t_s)** measurement.

4. The Invasive Weed Optimization (IWO) algorithm

The Invasive Weed Optimization (IWO) algorithm was offered by Mehrabian and Lucas in year 2006, which is taken from a widespread phenomenon in agriculture colonization of invasive weeds and named the algorithm Invasive Weed Optimization (IWO).

The IWO algorithm has the robustness, simple, effective, and also it is easy to understand and program. So far, it has been applied in many engineering fields.

A finite number of weeds are being dispread over the search area. The generated weeds are randomly distributed over the search space by normally distributed random numbers with a mean equal to zero. This process continues until the maximum number of weeds is reached. Only the weeds that have better fitness can survive and produce seeds, others are being eliminated. The process continues until the maximum iterations are reached [3,4,5,7].

IWO algorithm is a great gadget for finding a good and reasonable solutions for more complex problems among other algorithms because it has superior and distinguishing characteristics such as reproduction, spatial (diffusion) prevalence, and competitive exclusion. This algorithm has a good feature where it permits for all plants to participate in the regeneration process and there is a chance for the Weak plants to reproduce and if their seeds have a good finesse in the colony, they can survive. Another important feature of IWO is that weeds reproduce without mating. Each weed can produce new seeds, independently. This property adds a new attribute to the algorithm that each agent **(**Weed /plant**)** may have different number of variables during the optimization process. Thus, the number of variables can be chosen as one of the optimization parameters in this algorithm.

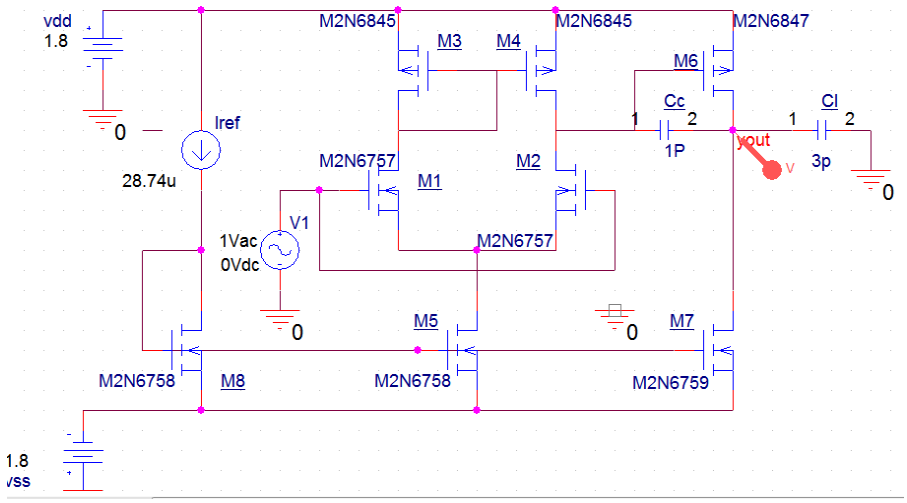

Figure .10. The practical circuit connected in common mode configuration used to calculate the value of CMRR

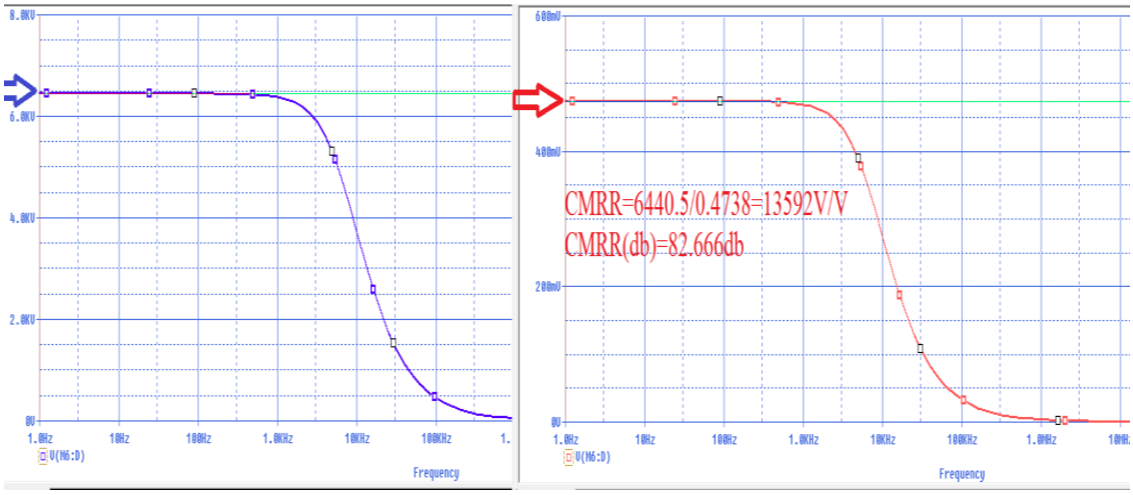

Figure .11. Simulation result of Common Mode Rejection Ratio (CMRR)

4.1. Definition of The Terms Used In IWO

- **Seed:** each unit in the colony which encompasses a value for each variable in the optimization problem before fitness evaluation.
- **Weed/Plant:** any seed that is evaluated grows to a weed or plant.
- **Fitness:** a value corresponding to the goodness of each unit after being evaluated.

4.2. Reproduction

A certain population of plants is allowed to produce seeds depending on its own and the colony's lowest and highest fitness, the number of seeds each plant produces increases linearly from the minimum possible seed production to its maximum level. The generated seeds are being randomly distributed over the dimensional search space by normally distributed random numbers with mean equal to zero; but varying variance. This step ensures that the produced seeds will be generated around the parent weed, leading to a local search around each plant.

If $\mathbf{W}_{ini}$ and $\mathbf{W}_f$ be the initial and final standard deviation and if $\boldsymbol{n}$ be a real number. Then the standard deviation for a particular iteration may be given as:

$$Wit = \left(\frac{itmax-it}{itmax}\right)^{n} (\mathbf{W}_{ini} - \mathbf{W}_f) + \mathbf{W}_f \quad (1)$$

where, $\boldsymbol{it}_{max}$ is the maximum number of iterations, $\mathbf{W}_{it}$ is the standard deviation at the present time step and $\boldsymbol{n}$ is the nonlinear modulation index. This step ensures that the probability of dropping a seed in a distant area decreases nonlinearly with iterations, which results in grouping fitter plants and elimination of inappropriate plants. Therefore, this is a selection mechanism of IWO [3,5,6,7]. The flowchart of IWO algorithm are given in Fig. 12 while the input parameters for the optimization process are presented in Table 4.

Table 4. Parameters of IWO used to optimize the Two Stage CMOS Op-Amp.

No.	Algorithm Parameters	Value	Parameters Definition
1	n_ini	5	Number of initial plants
2	itmax	100	Max number of iterations
3	dim	2	Dimension of the problem
4	plant_max_no	50	Max no. of plants
5	seedmax	5	Max number of seeds
6	seedmin	0	Min number of seeds
7	W_{ini}	1	Initial value of standard deviation
8	W_f	1e-7	Final value of standard deviation
9	n	3	Nonlinear modulation index

4.3. Optimization of proposed op-amp based on IWO algorithm

The Invasive Weed Optimization (IWO) algorithm can be used to optimize the proposed two stage CMOS op-amp. The idea of using IWO algorithm is to improve the performance parameters of CMOS Op-Amps specially power consumption and voltage gain. So the equations of power consumption and voltage gain must be written to IWO Algorithm to start the CMOS Op-Amp optimization which perform by using MATLAB program. When the program is running the IWO make a number of iterations determined by the user, and the output result can be identified and used in PSPICE program to give the minimum value for the power consumption and high value for voltage gain. This process can be repeated until getting the lower value of power consumption and high value of voltage gain and use it, and redesign the transistors with the new better dimensions.

$$P_{diss.} = (V_{DD} + |V_{SS}|) * (I_5 + I_6) \quad (2)$$

$$A_v = (2 * g_{m2} * g_{m6}) / [I_5 * (\lambda_2 + \lambda_4) * I_6 * (\lambda_7 + \lambda_6)] \quad (3)$$

$$\text{Fitness function} = (P_{diss} + 1/A_v) \quad (4)$$

After finished IWO algorithm which do with MATLAB (R2013b) program and get the improved results of power consumption and voltage gain based on new values of gate widths for MOSFET transistors and new value of (I_6), the new process parameters of CMOS op-amp obtained by IWO algorithm are sent to PSPICE program to evaluate the simulation results. Table 5 presents the transistor's aspect ratios based on IWO algorithm.

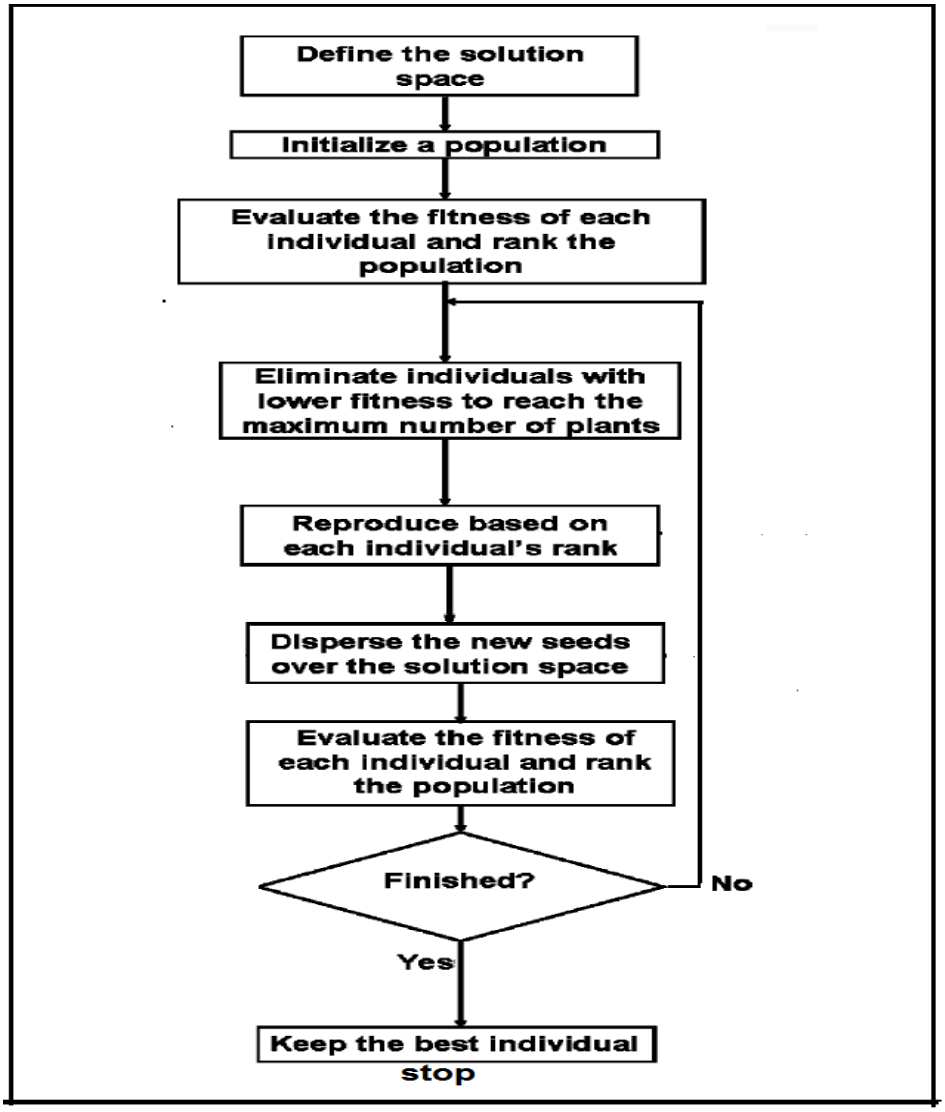

Figure .12. Flowchart of the Invasive Weed Optimization Algorithm.

Table 5. Transistor's aspect ratios for the two stage CMOS op-amp based on IWO algorithm.

No.	Transistor No.	Type	Gate Width W (μm)	Chanel length L(μm)
1	M1,2	N	10.42	0.18
2	M3,4	P	16.79	0.18
3	M5,8	N	0.68	0.18
4	M6	P	146.55	0.18
5	M7	N	2.98	0.18

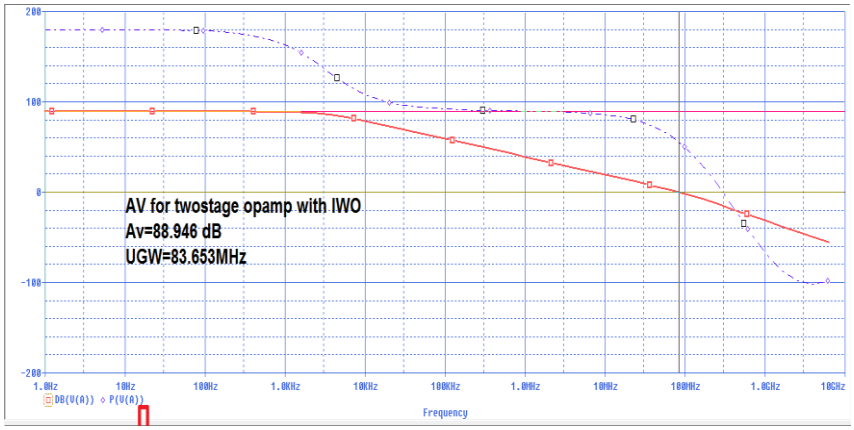

Figure .13. Simulation result of the frequency response (Gain measurement)

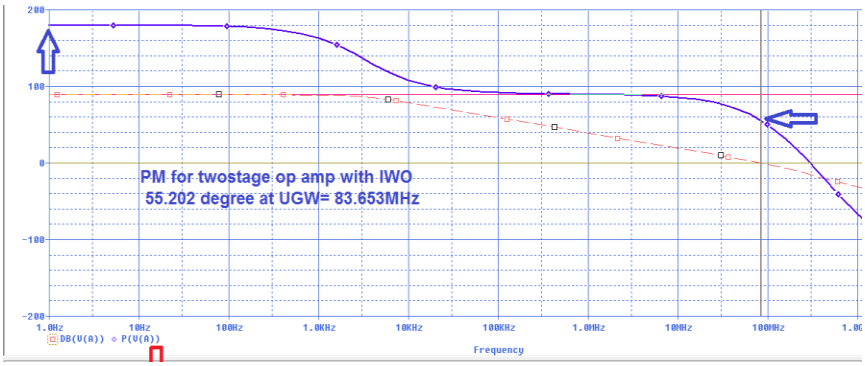

Figure .14. Simulation result of frequency response (phase measurement).

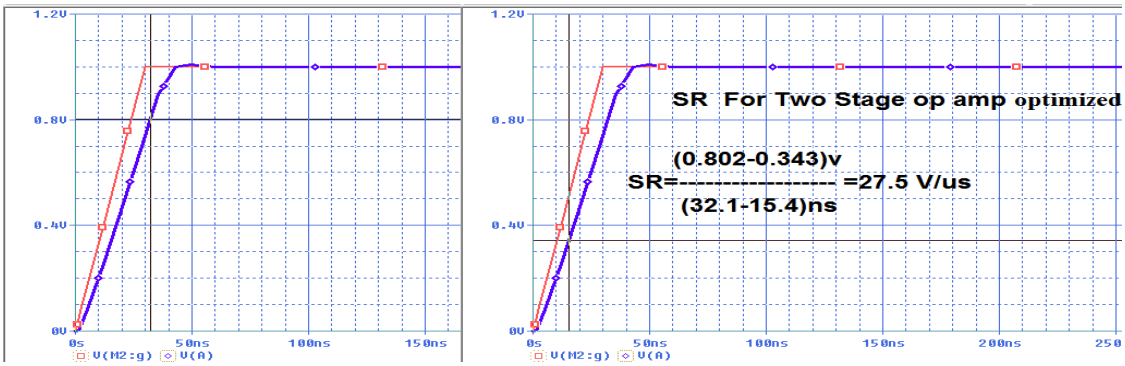

Figure .15. Simulation result of slew rate (SR) measurement

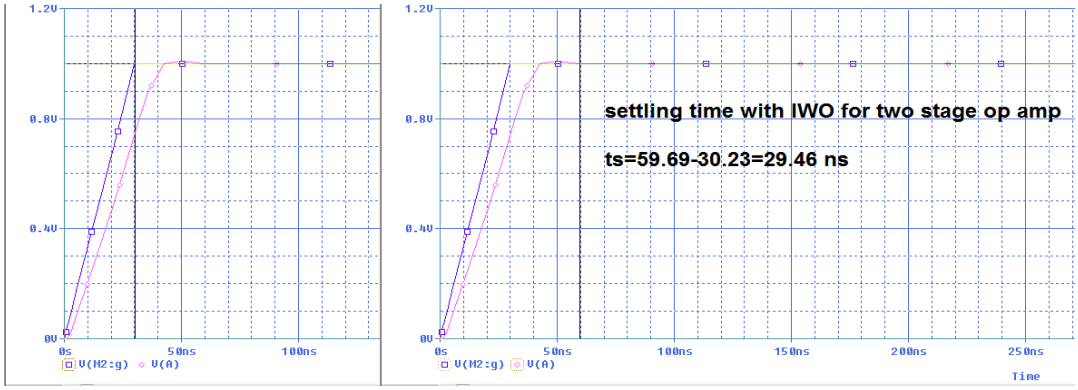

Figure .16. Simulation result of settling time measurement

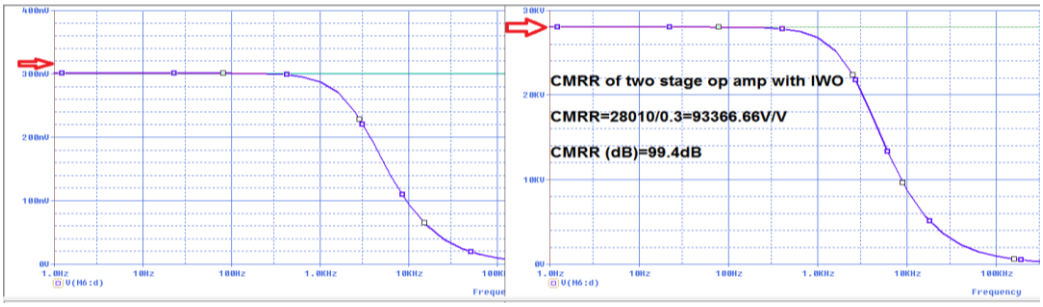

Figure .17. Simulation result of measurement Common Mode Rejection Ratio (CMRR)

Table 6. Comparison of the performance parameters for Two Stage CMOS Op-Amp with/without IWO algorithm.

No.	Performance Parameters	Without using IWO	With using IWO
1	DC Gain (dB)	76.178	88.946
2	Gain Bandwidth (MHz)	42.363	83.653
3	Phase Margin(degree)	60	55.202
4	Slew Rate(V/uS)	28	27.5
5	Settling time Ts (nS)	42.85	29.46
6	CMRR (dB)	82.666	99.4
7	Power dissipation (μW)	855	579.6

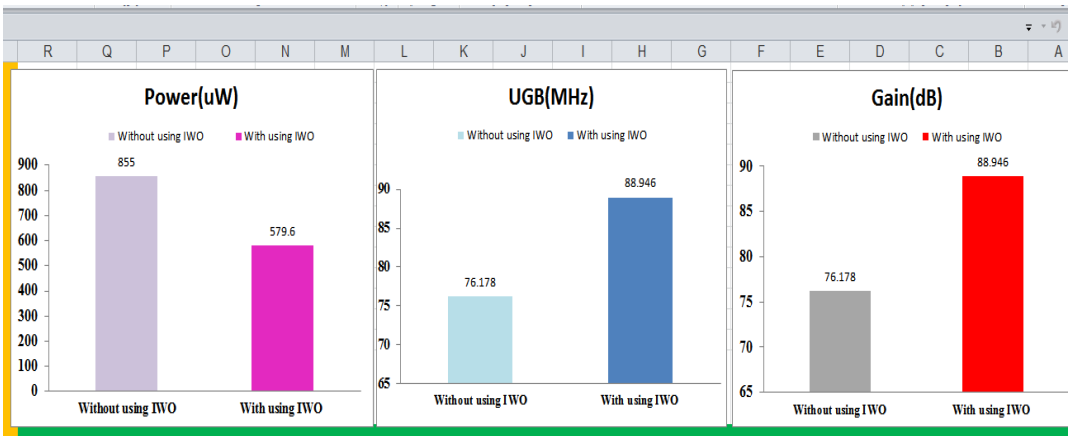

Figure .18. Comparison of the performance parameters (power, UGB, Gain) for Two Stage CMOS Op-Amp with & without using IWO.

The simulation results of the important performance parameters for the two-stage CMOS op-amp based on IWO algorithm are illustrated in Figs. 13-17. Table 6 summarizes a comparison of main performance parameters in two cases under study: with IWO and without IWO.

As presented in Fig. 18, it is seen that the value of DC voltage gain is 88.946 dB while the previous value of it without using IWO is 76.178 dB with increase about 17%, also the Gain Bandwidth Product (GBP) is 83.653MHz while the previous value is 42.363MHz that is mean it's value is doubled with IWO. When we speak about power dissipation we can say it's value decreased by 32% from 855μW to 579mW after optimization .Not that is all, there is another Parameters such as CMRR and Settling time (ts), these two parameters are also improved together, the CMRR from 82.666 dB to 99.4 dB, and the value of ts is change from 42.85nS to 29.46nS.

5. Conclusions

The significant progress in the manufacture of integrated circuits makes transistor performance greatly improved. Where we see today that the length of the channel length for a transistor of the type of MOS is very few and the limit of 45nm. This technological development has made transistor operate at high frequencies and low power consumption with very small chip area.

This matter is very important for the future works, especially with supply voltages becoming more limited, operational amplifier output swings becomes an extremely critical parameter, and also the power consumption is become very important parameter. So that the designers must be able to tradeoff or swapping among more than one important parameter.

Through the simulation results using PSPICE (version 16.6.0) based on 180nm TSMC technology obtained we conclude the following points:

1. The variation of load capacitor (C_L) effect on the value of GBP. Where the decreasing in load capacitor value increasing the value of GBP.

2. The use of the Invasive Weed Optimization (IWO) algorithm resulted in a significant improvement in the performance of the Two-Stage CMOS Op-Amp operation, where the GBP value multiplied by about 100% and the voltage gain increased around 17%, the power consumption decreased by 32% and CMRR increased by 20%.

3. The IWO algorithm is very efficient in improving the performance of the proposed CMOS Op-Amp and can be applied to the rest of the designs with the same working principle.

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